

**AMENDMENTS TO THE CLAIMS****PLEASE AMEND CLAIMS 1 to 15 AS FOLLOWS:**

1 1. ( Currently amended) A method of diagnosing a failure in a circuit in a  
2 complex semiconductor device utilizing logic circuits, formed of latches, that have  
3 failed functional testing comprising the steps of:  
4 selecting a semiconductor device having logic circuits formed of latches;  
5 testing the logic circuits in the device and locating a failing logic circuit in  
6 said device;  
7 selecting a functional test procedure;  
8 selecting a structural design and test technique;  
9 combining said with functional test procedure and said structural design and test  
10 techniques technique to dynamically create a new test pattern based on the  
11 functional located failure; and  
12 diagnosing the failing circuit to determine determine the location of and type of  
13 error in the said failing circuit.

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1 2. (Currently amended) The method of claim 1, wherein the step of said  
2 combining functional testing of the device circuitry with structural design and test  
3 techniques to dynamically create a new test pattern based on the functional failure  
4 includes the step of transforming a functional pattern into into a scan deterministic  
5 pattern.

1 3. (Currently amended) The method of claim 2, wherein the failing logic  
2 circuit device circuitry is diagnosed as stuck at zero.

1 4. (Currently amended) The method of claim 2, wherein the failing logic  
2 circuit device circuitry is diagnosed as stuck at one.

1 5. (Currently amended) The method of claim 2, wherein the failed logic  
2 circuit device circuitry has is diagnosed as having AC faults.

1 6. (Currently amended) The method of claim 2, wherein the failed logic  
2 circuit device circuitry has is diagnosed as having transitional faults.

1 7. ( Currently amended) A method of testing a complex semiconductor device  
2 by transforming a functional pattern into a scan determinative pattern utilizing scan  
3 chains and logic circuits, formed of latches, consisting of the steps of:  
4 selecting a first semiconductor device having a plurality of storage latches  
5 concatenated in a scan chain that includes embedded circuit memories;  
6 performing a functional test, comprised consisting of a selected number of test  
7 cycles, on said semiconductor device;  
8 identifying any failure a failing latch in a logic circuit in the scan chain during the  
9 functional test;  
10 unloading the values of all the latches from the scan chain before the identified  
11 failing latch failure may include reading the embedded circuit memories and other  
12 circuit storage elements;  
13 generating a Load from the unloaded states of the latches; values of all the latches  
14 from the scan chain before the identified failing latch;  
15 selecting a second correctly operating semiconductor device having a plurality of  
16 storage latches concatenated in a scan chain identical to said first device;  
17 applying the generated Load which as the first event of a newly created independent  
18 an LSSD deterministic pattern by using the same identical primary inputs and Clocks  
19 that produced the failure to in said failing latch in said first semiconductor device to  
20 said second semiconductor known correctly operating device using a the  
21 bootstrapping technique;

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22 and unloading the output of said second semiconductor device the correctly operating  
23 device to generate a deterministic LSSD pattern; and operating applying the generated  
24 deterministic LSSD pattern to the failing device and  
25 diagnosing the failure using existing LSSD deterministic tools.

1 8. (Currently amended) The method of claim 3 7, wherein said scan chain  
2 chains are is an LSSD scan chain chains and said created independent deterministic  
3 pattern is an patterns are LSSD deterministic patterns: pattern.

1 9. (Currently amended) The method of claim 3 7, wherein said scan chain  
2 chains are is a GSD scan chain chains and said created independent deterministic  
3 pattern is a patterns are is a GSD deterministic patterns: pattern.

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1 10. ( Currently amended) A method of diagnosing a complex semiconductor  
2 device utilizing logic circuits, formed of latches, ~~that have failed functional testing~~  
3 comprising the steps of:  
4 subjecting a first semiconductor device, having embedded sequential logic circuits  
5 and storage circuits including a plurality of latches arranged in a LSSD scan chain to  
6 a test that consists of applying a plurality of primary inputs and clock signals to said  
7 device;  
8 identifying a failing vector of the failed latch in a logic circuit in said scan chain  
9 during functional said test;  
10 observing the states of the logic circuit containing said failed latch device by  
11 unloading the values of the plurality of latches from the LSSD scan chain  
12 positioned in said scan chain before the failing vector identified failed latch which  
13 may include reading any the embedded circuit memories and other circuit storage  
14 elements positioned in said scan chain before the failed latch  
15 generating a LOAD from the unloaded states of the latches positioned in said scan  
16 chain before the failed latch;  
17 applying the generated LOAD which as the first event of a newly created  
18 independent LSSD deterministic pattern by using the same identical primary inputs  
19 and Clocks signals identical to the primary inputs and clock signals that produced  
20 the failure to a known, correctly operating, device utilizing logic circuits formed of a  
21 plurality of latches arranged in a LSSD scan chain and a plurality of other storage

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22        elements identical to said failed device by applying a plurality of primary inputs and  
23        clock signals to said device by using a the bootstrapping technique; and  
24        unloading the output of the correctly operating device to generate a deterministic  
25        LSSD pattern; and  
26        operating the generated deterministic LSSD pattern to the failing device; and  
27        diagnosing the failure using existing LSSD deterministic tools.

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1 11. (Currently amended) The method of claim 6, 10, wherein said scan chains  
2 are GSD scan chains and said created Independent deterministic patterns are GSD  
3 deterministic patterns.

1 12. (Canceled) A method of diagnosing a complex semiconductor device utilizing logic  
2 circuits, formed of latches, that have failed functional testing comprising the steps of:  
3 combining functional testing of the device circuitry with structural design  
4 and test techniques to dynamically create new test patterns based on the functional  
5 failure; and  
6 determining the location of and type of error in the failing circuit.

1 13. (Currently amended) The method of claim 1 wherein the step of said  
2 combining functional testing of the device circuitry with structural design and test  
3 techniques to dynamically  
4 create new test patterns based on the functional diagnosed failure includes the step of  
5 transforming functional patterns into scan deterministic patterns.

1 14. (Cancelled) A testing protocol for determining whether any of the internal  
2 functional circuit elements in a complex solid state device is stuck, comprising the  
3 steps of:  
4 applying a predetermined set of functional vectors have been applied thus allowing  
5 functional patterns to a solid state device;  
6 allowing the set of device run at speed until the failing point is reached;  
7 unloading the data from said device state of the machine; and Isolating the fault.

1 15. (Currently amended) The testing protocol of claim 8 wherein the scan access  
2 initializes initializes the internal state of the device prior to applying the functional  
3 patterns a predetermined set of functional vectors to narrow the  
4 partition of the functional patterns; and  
5 iteratively executing multiple partitions to said set of functional vectors to  
6 ultimately yield one or more independent scan test vectors.